LM4844 Boomer® Audio Power Amplifier Series
Stereo 1.2W Audio Sub-System with 3D Enhancement

General Description

The LM4844 is an integrated audio sub-system designed for stereo cell phone applications. Operating on a 3.3V supply, it combines a stereo speaker amplifier delivering 495mW per channel into an 8Ω load and a stereo OCL headphone amplifier delivering 33mW per channel into a 32Ω load.

It integrates the audio amplifiers, volume control, mixer, power management control, and National 3D enhancement all into a single package. In addition, the LM4844 routes and mixes the stereo and mono inputs into 10 distinct output modes. The LM4844 is controlled through an I²C compatible interface.

Boomer audio power amplifiers are designed specifically to provide high quality output power with a minimal amount of external components.

The LM4844 is available in a very small 2.5mm x 2.9mm 30-bump micro SMD (TL) package.

Key Specifications

■ P_{OUT}, Stereo BTL, 8Ω, 3.3V, 1% THD+N	495mW (typ)
■ P_{OUT} HP, 32Ω, 3.3V, 1% THD+N	33mW (typ)
■ Shutdown Current, 3.3V	0.1µA (typ)

Features

- Stereo speaker amplifier
- Stereo OCL headphone amplifier
- Independent Left, Right, and Mono volume controls
- National 3D enhancement
- I²C compatible interface
- Ultra low shutdown current
- Click and Pop Suppression circuit
- 10 distinct output modes

Applications

- Cell Phones
- PDAs
- Portable Gaming Devices
- Internet Appliances
- Portable DVD, CD, AAC, and MP3 Players

Block Diagram

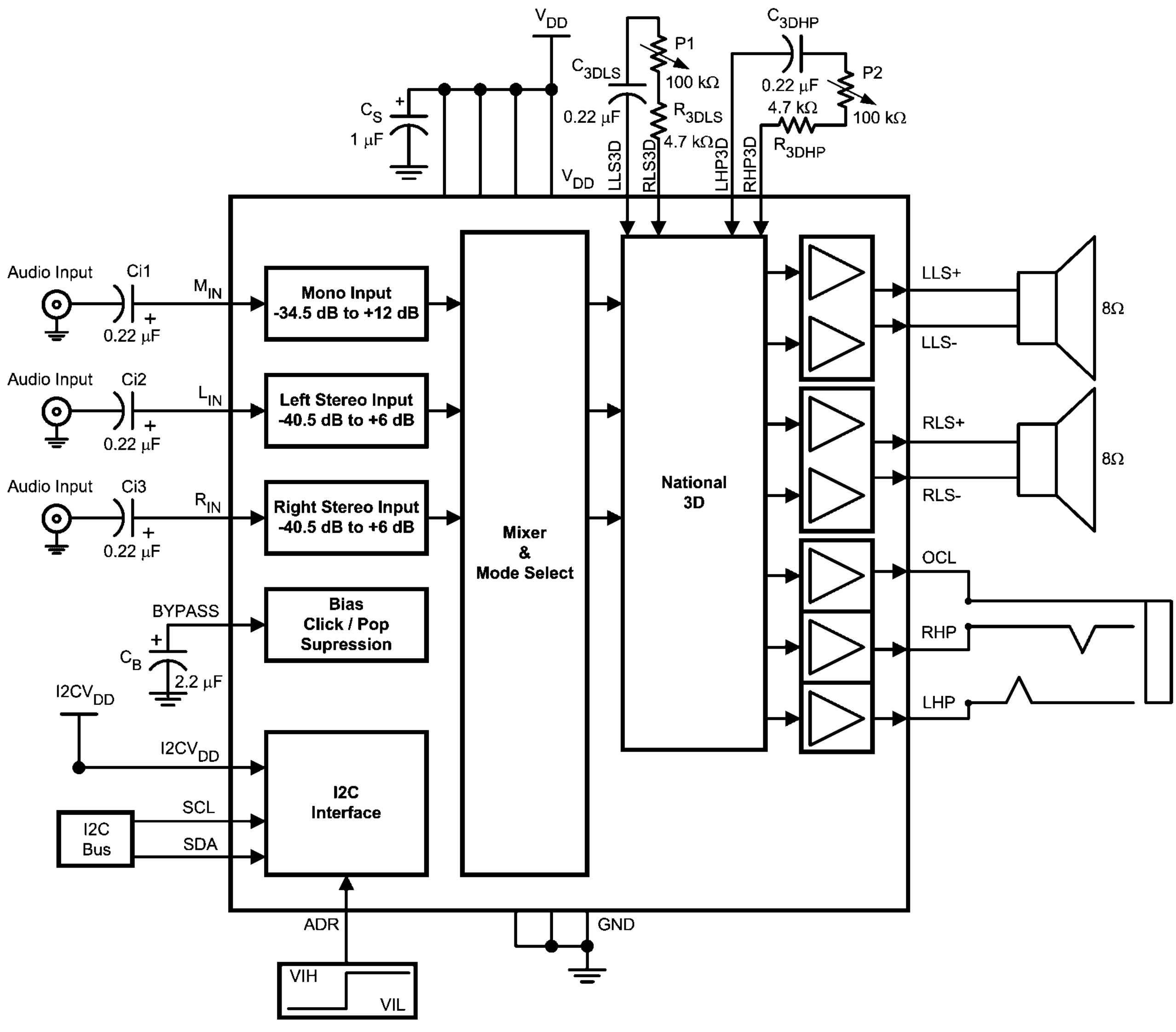
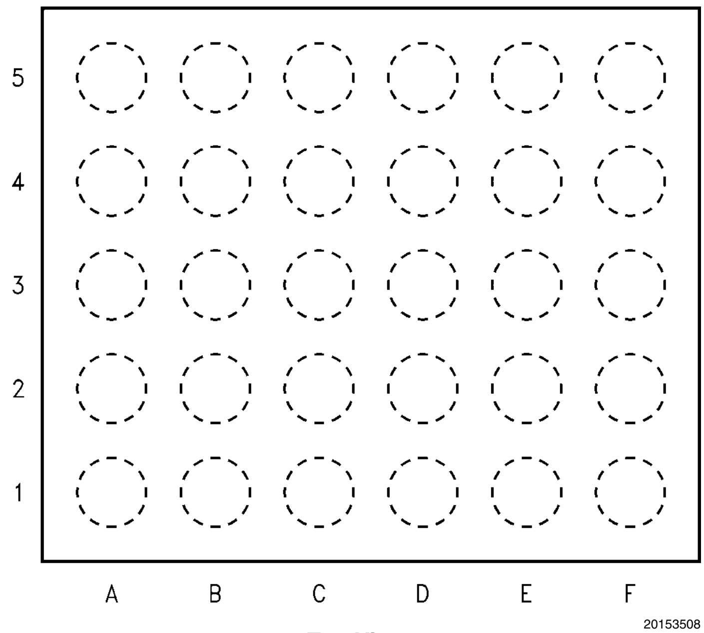


FIGURE 1. Audio Sub-System Block Diagram

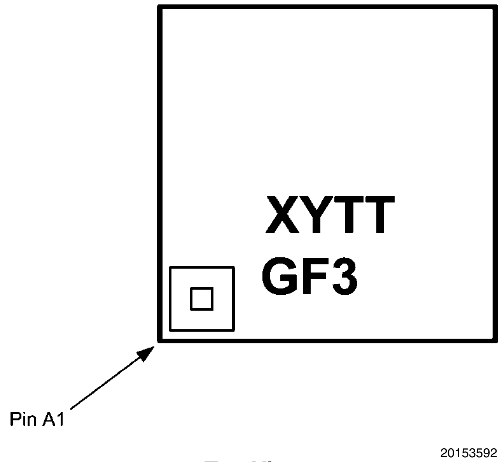
Connection Diagrams

30 Bump Micro SMD (TL) Package



Top View
(Bump-side down)
Order Number LM4844TL
See NS Package Number TLA30CZA

Micro SMD (TL) Marking



Top View
XY = 2 Digit Date Code
TT = Die Traceability
G = Boomer Family
F3 = LM4844TL

Pin Connection (TL)

Pin	Name	Pin Description
A1	RLS+	Right Loudspeaker Positive Output
A2	V_{DD}	Power Supply
A3	SDA	Data
A4	RHP3D	Right Headphone 3D
A5	RHP	Right Headphone Output
B1	GND	Ground
B2	I^2CV_{DD}	I^2C Interface Power Supply
B3	ADR	I^2C Address Select
B4	LHP3D	Left Headphone 3D
B5	V_{DD}	Power Supply
C1	RLS-	Right Loudspeaker Negative Output
C2	NC	No Connect
C3	SCL	Clock
C4	NC	No Connect
C5	GND	Ground
D1	LLS-	Left Loudspeaker Negative Output
D2	V_{DD}	Power Supply
D3	M_{IN}	Mono Input
D4	NC	No Connect
D5	OCL	V_{DD}/2 Supply for headphone jack's sleeve
E1	GND	Ground
E2	BYPASS	Half-supply bypass
E3	LLS3D	Left Loudspeaker 3D
E4	R_{IN}	Right Stereo Input
E5	NC	No Connect
F1	LLS+	Left Loudspeaker Positive Output
F2	V_{DD}	Power Supply
F3	RLS3D	Right Loudspeaker 3D
F4	L_{IN}	Left Stereo Input
F5	LHP	Left Headphone Output

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	−65°C to +150°C
Input Voltage	−0.3V to V_{DD} +0.3V
Power Dissipation (Note 3)	Internally Limited
ESD Susceptibility (Note 4)	2000V
ESD Susceptibility (Note 5)	200V
Junction Temperature (T_J)	150°C
Thermal Resistance	
θ_{JA} (TLA30CZA)	62°C/W

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage (V_{DD})	$2.7V \le V_{DD} \le 5.5V$
Supply Voltage (I^2CV_{DD}) (Note 10)	$I^2CV_{DD} \le V_{DD}$ $1.7V \le I^2CV_{DD} \le 5.5V$

Audio Amplifier Electrical Characteristics V_{DD} = 5.0V (Notes 1, 2)

The following specifications apply for V_{DD} = 5.0V, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4844		Units (Limits)
			Typical (Note 6)	Limits (Notes 7, 8)	
I_{DD}	Supply Current	V_{IN} = 0V, No load; LD5 = RD5 = 0			
		Mode 4, 9, 14	5	8	mA (max)
		Mode 2, 7, 12	12	18	mA (max)
		Mode 3, 8, 13	13	20	mA (max)
I_{SD}	Shutdown Current	Mode 0	0.2	2.5	µA (max)
P_O	Output Power	Speaker; THD+N = 1%; f = 1kHz; 8Ω BTL	1.2	0.9	W (min)
		Headphone; THD+N = 1%; f = 1kHz; 32Ω SE	80	60	mW (min)
THD+N	Total Harmonic Distortion Plus Noise	LD5 = RD5 = 0			
		Speaker; P_O = 400mW; f = 1kHz; 8Ω BTL	0.05		%
		Headphone; P_O = 15mW; f = 1kHz; 32Ω SE	0.06		%
V_{OS}	Offset Voltage	Speaker; LD5 = RD5 = 0	5	40	mV (max)
		Headphone; LD5 = RD5 = 0	2	30	mV (max)
N_{OUT}	Output Noise	A-weighted, 0dB gain; LD5 = RD5 = 0			
		Speaker; Mode 2, 3, 7, 8	31		µV
		Speaker; Mode 12, 13	35		µV
		Headphone; Mode 3, 4, 8, 9	12		µV
		Headphone; Mode 13, 14	14		µV
PSRR	Power Supply Rejection Ratio	f = 217Hz; V_{rip} = 200mV_{pp}; C_B = 2.2µF; 0dB Gain Setting; LD5 = RD5 = 0			
		Speaker; Mode 2, 3, 7, 8	71		dB
		Speaker; Mode 12, 13,	65	55	dB (min)
		Headphone; Mode 3, 4, 8, 9	76		dB
		Headphone; Mode 13, 14	72	62	dB (min)
Xtalk	Crosstalk	LD5 = RD5 = 0			
		Loudspeaker; P_O = 400mW; f = 1kHz	84		dB
		Headphone; P_O = 15mW; f = 1kHz	60		dB
T_{WU}	Wake-up Time	CD4 = 0; C_B = 2.2µF	103		ms
		CD4 = 1; C_B = 2.2µF	42		ms

Audio Amplifier Electrical Characteristics V_{DD} = 3.0V (Notes 1, 2)

The following specifications apply for V_{DD} = 3.0V, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4844		Units (Limits)
			Typical (Note 6)	Limits (Notes 7, 8)	
I_{DD}	Supply Current	V_{IN} = 0V, No load; LD5 = RD5 = 0			
		Mode 4, 9, 14	4.5	7.5	mA (max)
		Mode 2, 7, 12	10	16	mA (max)
		Mode 3, 8, 13	11	18	mA (max)
I_{SD}	Shutdown Current	Mode 0	0.1	2	µA (max)
P_O	Output Power	Speaker; THD+N = 1%; f = 1kHz; 4Ω BTL	390	320	mW (min)
		Headphone; THD+N = 1%; f = 1kHz; 32Ω SE	28	21	mW (min)
THD+N	Total Harmonic Distortion Plus Noise	LD5 = RD5 = 0			
		Speaker; P_O = 200mW; f = 1kHz; 8Ω BTL	0.05		%
		Headphone; P_O = 10mW; f = 1kHz; 32Ω SE	0.05		%
V_{OS}	Offset Voltage	Speaker; LD5 = RD5 = 0	5	40	mV (max)
		Headphone; LD5 = RD5 = 0	2	30	mV (max)
N_{OUT}	Output Noise	A-weighted; 0dB gain; LD5 = RD5 = 0			
		Speaker; Mode 2, 3, 7, 8	32		µV
		Speaker; Mode 12, 13	41		µV
		Headphone; Mode 3, 4, 8, 9	13		µV
		Headphone; Mode 13, 14	15		µV
PSRR	Power Supply Rejection Ratio	f = 217Hz, V_{rip} = 200mV_{pp}; C_B = 2.2µF; 0dB Gain Setting; LD5 = RD5 = 0			
		Speaker; Mode 2, 3, 7, 8	73		dB
		Speaker; Mode 12, 13,	66	55	dB (min)
		Headphone; Mode 3, 4, 8, 9	78		dB
		Headphone; Mode 13, 14	72	62	dB (min)
Xtalk	Crosstalk	LD5 = RD5 = 0			
		Loudspeaker; P_O = 200mW; f = 1kHz	85		dB
		Headphone; P_O = 10mW; f = 1kHz	60		dB
T_{WU}	Wake-up Time	CD4 = 0; C_B = 2.2µF	70		ms
		CD4 = 1; C_B = 2.2µF	30		ms

Volume Control Electrical Characteristics (Notes 1, 2)

The following specifications apply for 3V ≤ V_{DD} ≤ 5V and 3V ≤ I^2CV_{DD} ≤ 5V, unless otherwise specified. Limits apply for T_A = 25° C.

Symbol	Parameter	Conditions	LM4844		Units (Limits)
			Typical (Note 6)	Limits (Notes 7, 8)	
	Stereo Volume Control Range	maximum gain setting	6	5.5 6.5	dB (min) dB (max)
		minimum gain setting	-40.5	-41 -40	dB (min) dB (max)
	Mono Volume Control Range	maximum gain setting	12	11.5 12.5	dB (min) dB (max)
		minimum gain setting	-34.5	-35 -34	dB (min) dB (max)
	Volume Control Step Size		1.5		dB
	Volume Control Step Size Error		+/-0.2	+/-0.5	dB (max)
	Stereo Channel to Channel Gain Mismatch		0.3		dB
	Mute Attenuation	Mode 12, V_{in} = 1V_{RMS}			
		Headphone	100		dB
	L_{IN} and R_{IN} Input Impedance	maximum gain setting	33	25 42	kΩ (min) kΩ (max)
		minimum gain setting	100	75 125	kΩ (min) kΩ (max)
	M_{IN} Input Impedance	maximum gain setting	20	15 25	kΩ (min) kΩ (max)
		minimum gain setting	96	73 123	kΩ (min) kΩ (max)

Control Interface Electrical Characteristics (Notes 1, 2)

The following specifications apply for V_{DD} = 5.0V and 3.0V, T_A = 25°C, 2.2V ≤ I^2CV_{DD} ≤ 5.5V, unless otherwise specified.

Symbol	Parameter	Conditions	LM4844		Units (Limits)
			Typical (Note 6)	Limits (Notes 1, 7, 8)	
t_1	I²C Clock Period			2.5	μs (min)
t_2	I²C Data Setup Time			100	ns (min)
t_3	I²C Data Stable Time			0	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition time			100	ns (min)
t_6	I²C Data Hold Time			100	ns (min)
V_{IH}	I²C Input Voltage High			0.7 x I^2CV_{DD}	V (min)
V_{IL}	I²C Input Voltage Low			0.3 x I^2CV_{DD}	V (max)

Control Interface Electrical Characteristics (Notes 1, 2)

The following specifications apply for V_{DD} = 5.0V and 3.0V, T_A = 25°C, 1.7V ≤ I^2CV_{DD} ≤ 2.2V, unless otherwise specified.

Symbol	Parameter	Conditions	LM4844		Units (Limits)
			Typical (Note 6)	Limits (Notes 1, 7, 8)	
t_1	I²C Clock Period			2.5	μs (min)
t_2	I²C Data Setup Time			250	ns (min)
t_3	I²C Data Stable Time			0	ns (min)

Symbol	Parameter	Conditions	LM4844		Units (Limits)
			Typical (Note 6)	**Limits** (Notes 1, 7, 8)	
t_4	Start Condition Time			250	ns (min)
t_5	Stop Condition time			250	ns (min)
t_6	I^2C Data Hold Time			250	ns (min)
V_{IH}	I^2C Input Voltage High			0.7 x I^2CV_{DD}	V (min)
V_{IL}	I^2C Input Voltage Low			0.25 x I^2CV_{DD}	V (max)

Note 1: All voltages are measured with respect to the GND pin unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4844 typical application with V_{DD} = 3.3V and R_L = 8Ω stereo operation, the total power dissipation is TBDW. θ_{JA} = TBD°C/W.

Note 4: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 5: Machine Model, 220pF-240pF discharged through all pins.

Note 6: Typicals are measured at +25°C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

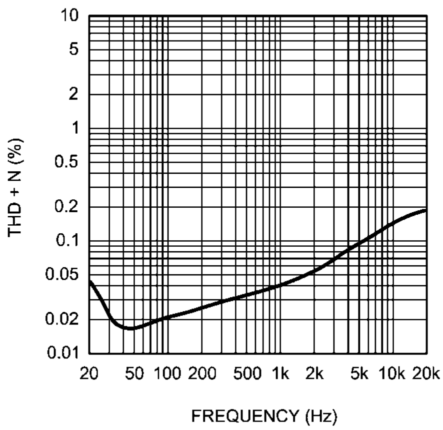
Note 8: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Note 9: Shutdown current and supply current are measured in a normal room environment.

Note 10: Refer to Control Interface Electrical Characteristics tables on page 6.

Typical Performance Characteristics

LM4844TL THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, Mode 7
LS, P_O = 400mW



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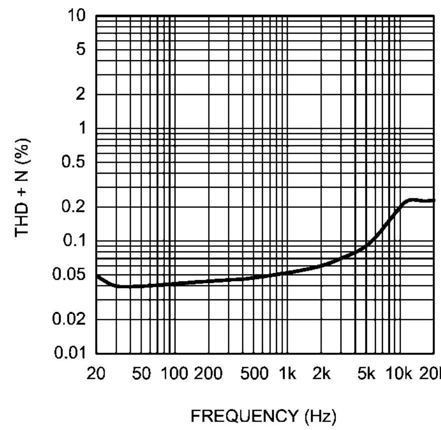
LM4844TL THD+N vs Frequency
V_{DD} = 3V, R_L = 8Ω, Mode 7
LS, P_O = 200mW



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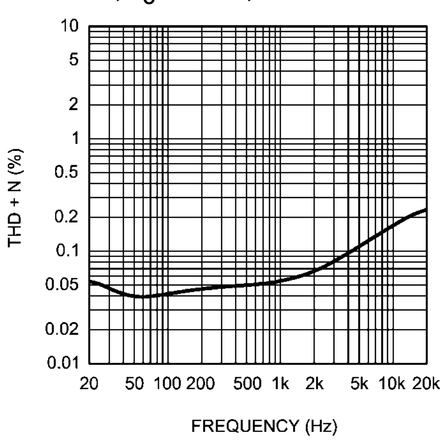
LM4844TL THD+N vs Frequency
V_{DD} = 5V, R_L = 32Ω, Mode 9
HP, P_O = 15mW, 0dB Gain



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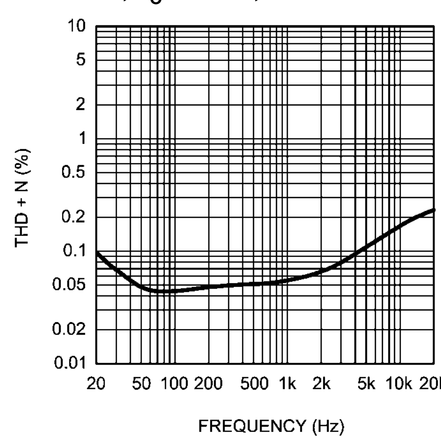
LM4844TL THD+N vs Frequency
V_{DD} = 3V, R_L = 32Ω, Mode 9
HP, P_O = 10mW, 0dB Gain



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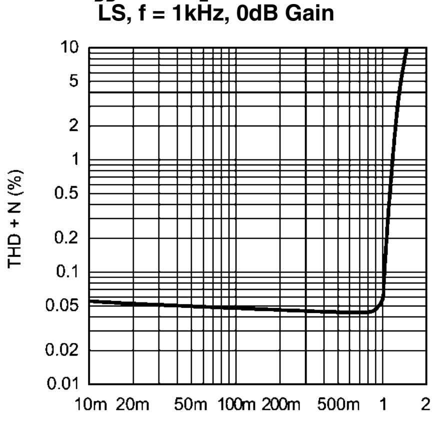
LM4844TL THD+N vs Output Power
V_{DD} = 5V, R_L = 8Ω, Mode 7
LS, f = 1kHz, 0dB Gain



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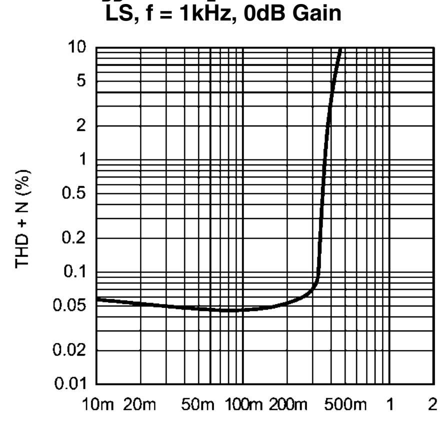
LM4844TL THD+N vs Output Power
V_{DD} = 3V, R_L = 8Ω, Mode 7
LS, f = 1kHz, 0dB Gain



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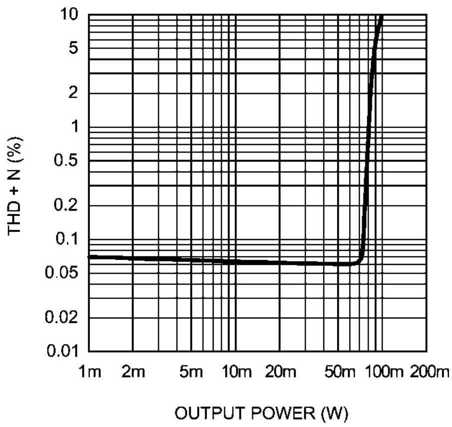
LM4844TL THD+N vs Output Power
V_{DD} = 5V, R_L = 32Ω, Mode 9
HP, f = 1kHz, 0dB Gain



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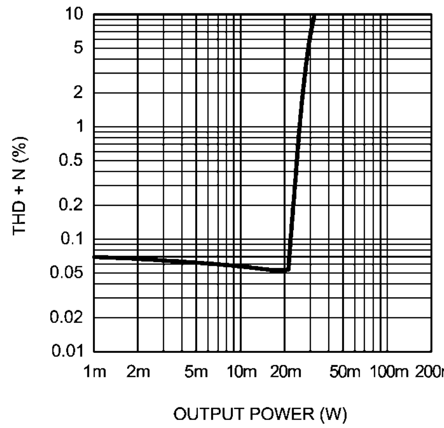
LM4844TL THD+N vs Output Power
V_{DD} = 3V, R_L = 32Ω, Mode 9
HP, f = 1kHz, 0dB Gain



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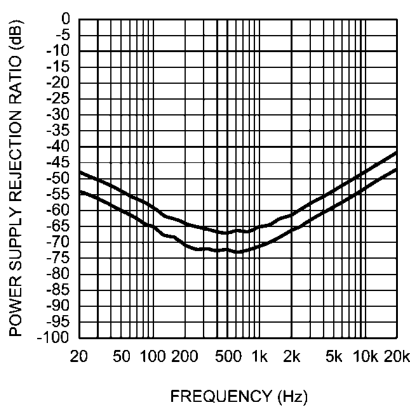
LM4844TL PSRR vs Frequency
V_{DD} = 5V, R_L = 8Ω, LS
Top-Modes 12, 13
Bottom-Modes 2, 3, 7, 8



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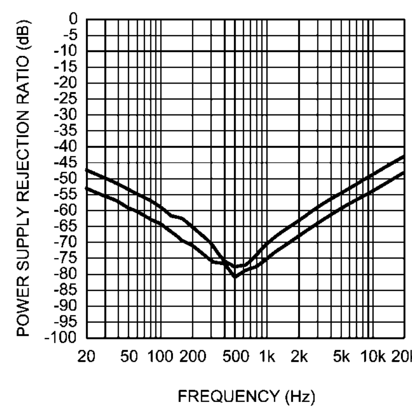
LM4844TL PSRR vs Frequency
V_{DD} = 3V, R_L = 8Ω, LS
Top-Modes 12, 13
Bottom-Modes 2, 3, 7, 8



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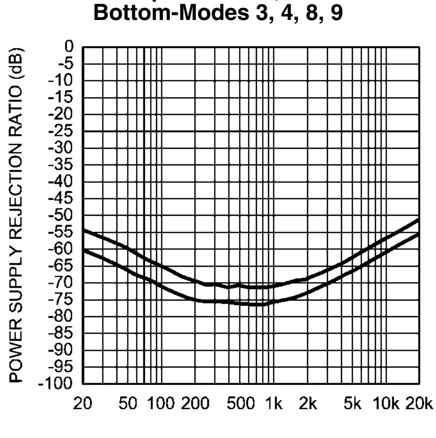
LM4844TL PSRR vs Frequency
V_{DD} = 5V, R_L = 32Ω, HP
Top-Modes 13, 14
Bottom-Modes 3, 4, 8, 9



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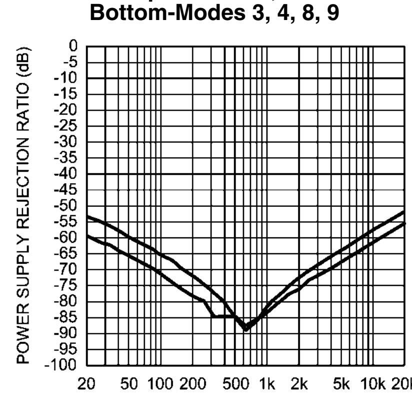
LM4844TL PSRR vs Frequency
V_{DD} = 3V, R_L = 32Ω, HP
Top-Modes 13, 14
Bottom-Modes 3, 4, 8, 9



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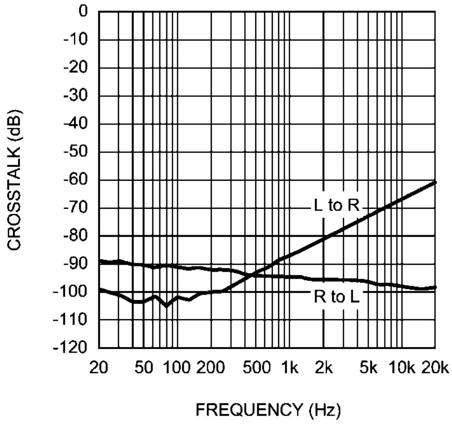
LM4844TL Crosstalk vs Frequency
V_{DD} = 5V, R_L = 8Ω, Mode 7
LS, P_O = 400mW



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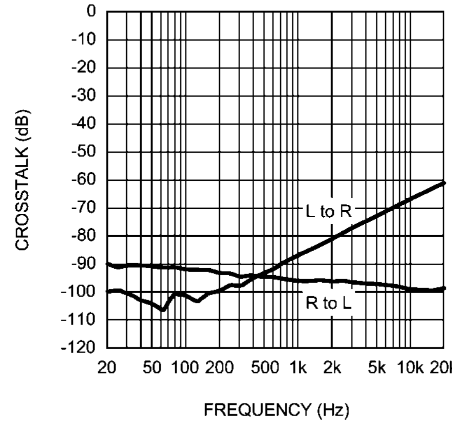
LM4844TL Crosstalk vs Frequency
V_{DD} = 3V, R_L = 8Ω, Mode 7
LS, P_O = 200mW



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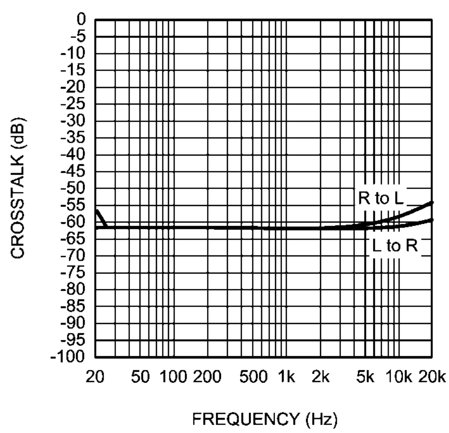
LM4844TL Crosstalk vs Frequency
V_{DD} = 5V, R_L = 32Ω, Mode 9
HP, P_O = 15mW, 0dB Gain



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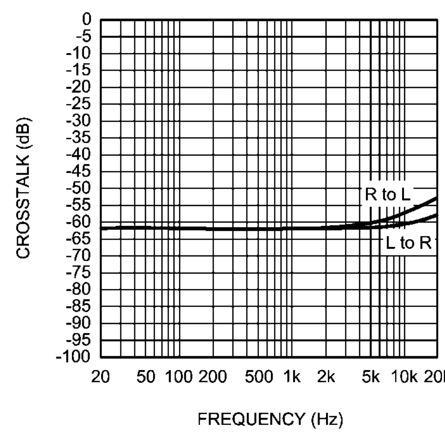
LM4844TL Crosstalk vs Frequency
V_{DD} = 3V, R_L = 32Ω, Mode 9
HP, P_O = 10mW, 0dB Gain



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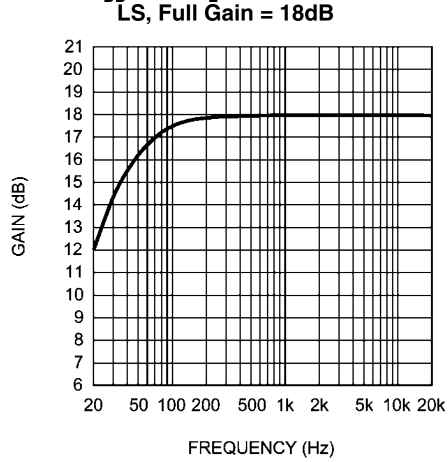
LM4844TL Frequency Response
V_{DD} = 5V, R_L = 8Ω, Mode 2
LS, Full Gain = 18dB



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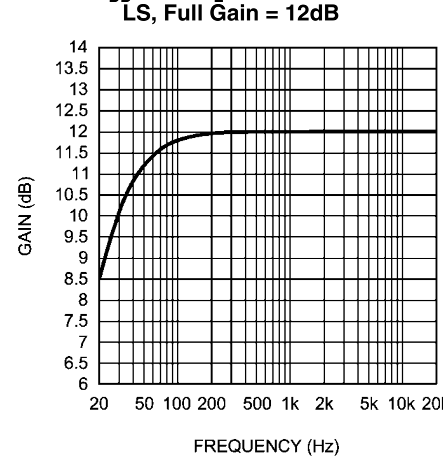
LM4844TL Frequency Response
V_{DD} = 5V, R_L = 8Ω, Mode 7
LS, Full Gain = 12dB



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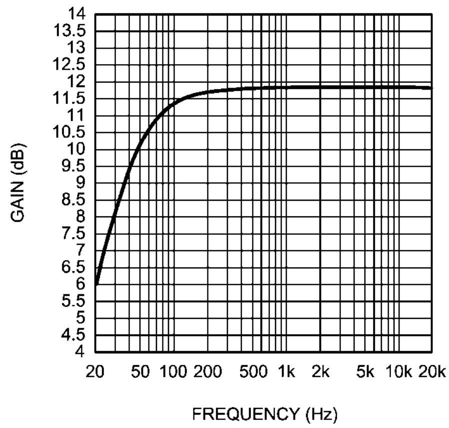
LM4844TL Frequency Response
V_{DD} = 5V, R_L = 32Ω, Mode 4
HP, Full Gain = 12dB



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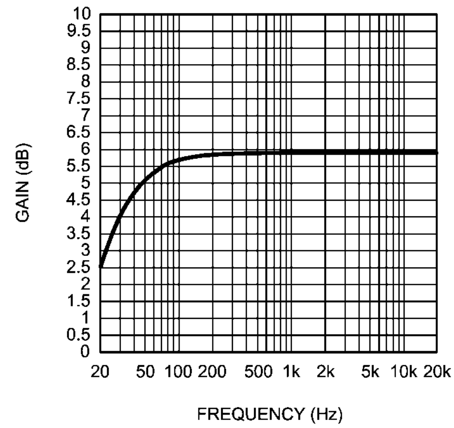
LM4844TL Frequency Response
V_{DD} = 5V, R_L = 32Ω, Mode 9
HP, Full Gain = 6dB



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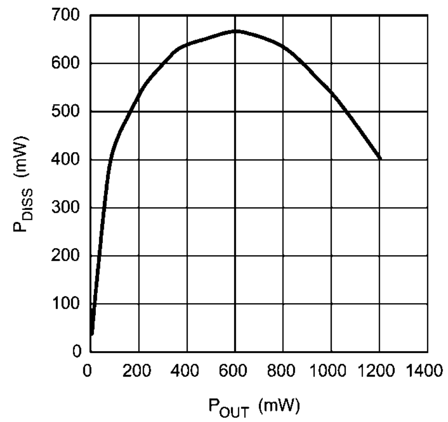
LM4844TL Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 8Ω
LS, per channel



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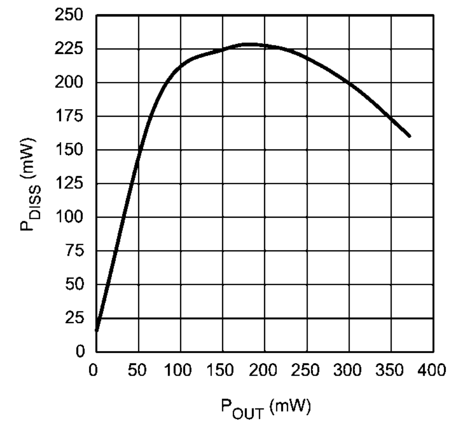
LM4844TL Power Dissipation vs Output Power
V_{DD} = 3V, R_L = 8Ω
LS, per channel



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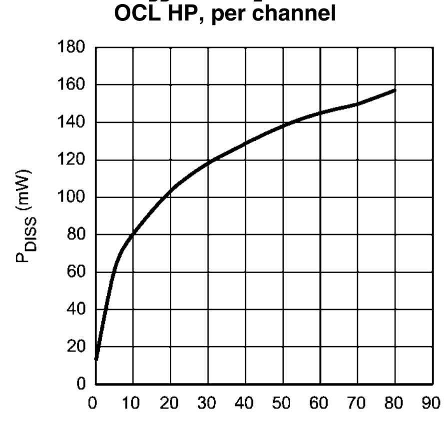
LM4844TL Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 8Ω
OCL HP, per channel



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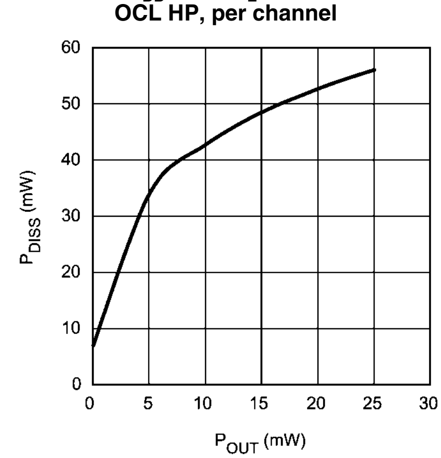
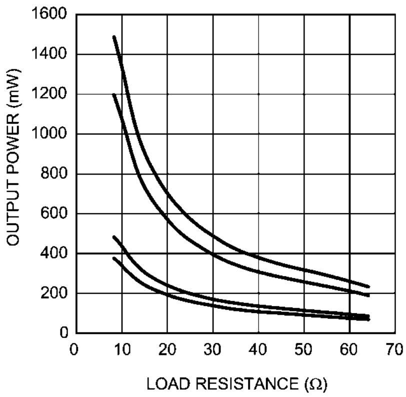
LM4844TL Power Dissipation vs Output Power
V_{DD} = 3V, R_L = 32Ω
OCL HP, per channel



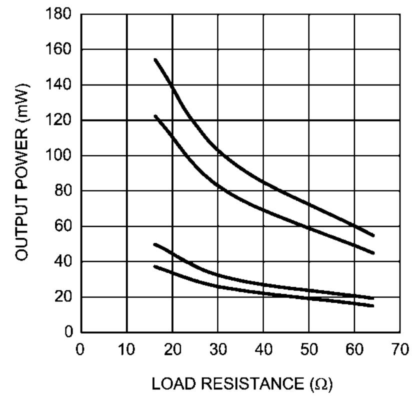
20153586

LM4844TL Output Power vs Load Resistance, LS
Top-V_{DD} = 5V, 10% THD+N; Topmid-V_{DD} = 5V, 1%THD+N
Botmid-V_{DD} = 3V, 10% THD+N;
Botmid-V_{DD} = 3V, 1% THD+N



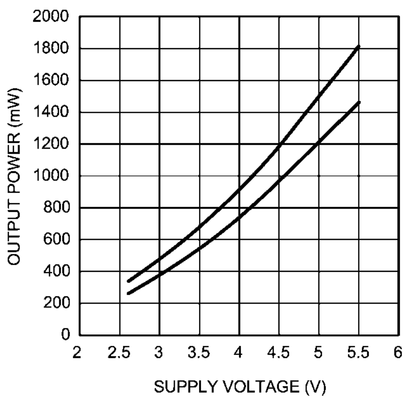
20153587

LM4844TL Output Power vs Load Resistance, HP
Top-V_{DD} = 5V, 10% THD+N; Topmid-V_{DD} = 5V, 1%THD+N
Botmid-V_{DD} = 3V, 10% THD+N;
Botmid-V_{DD} = 3V, 1% THD+N



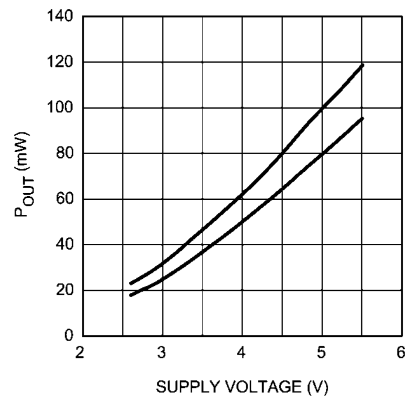
20153588

LM4844TL Output Power vs Supply Voltage, LS
R_L = 8Ω; Top- 10%THD+N , Bot- 1%THD+N



20153589

LM4844TL Output Power vs Supply Voltage, HP
R_L = 32Ω; Top- 10%THD+N, Bot- 1%THD+N



20153590

Application Information

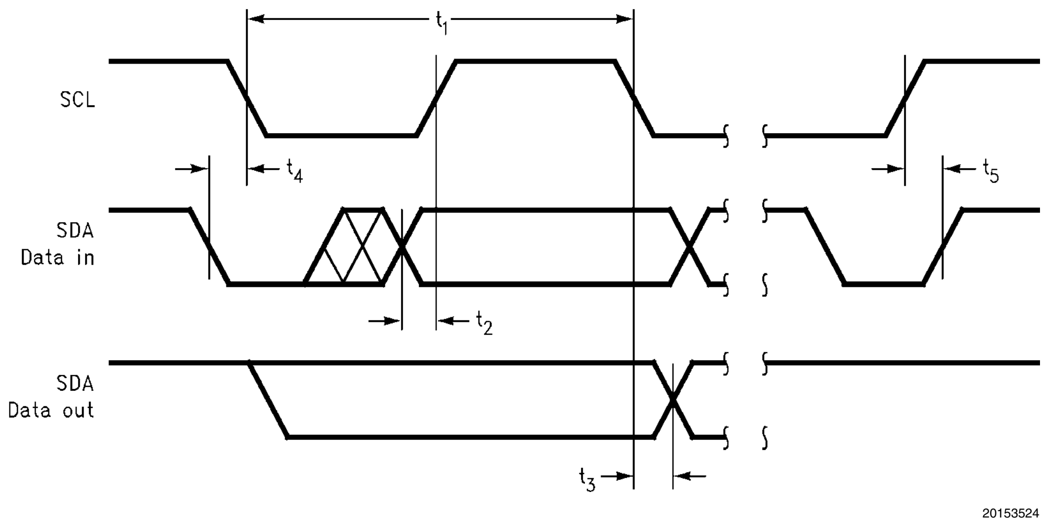


FIGURE 2. I²C Timing Diagram

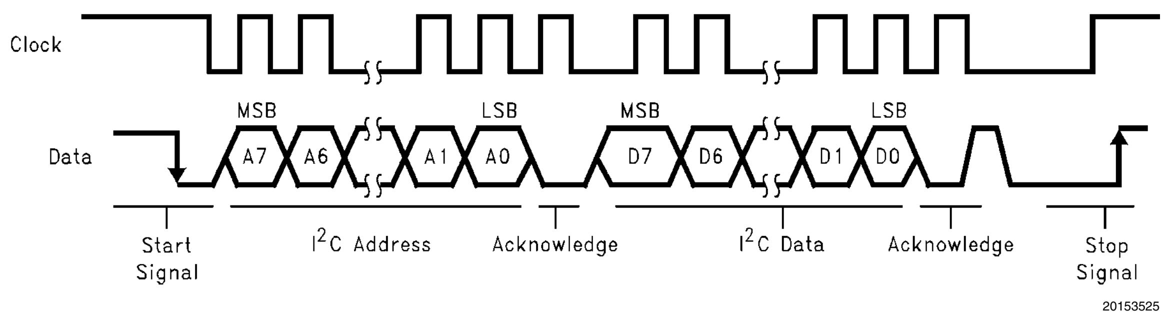


FIGURE 3. I²C Bus Format

TABLE 1. Chip Address

	A7	A6	A5	A4	A3	A2	A1	A0
Chip Address	1	1	1	1	1	0	EC	0
ADR = 0	1	1	1	1	1	0	0	0
ADR = 1	1	1	1	1	1	0	1	0

EC - externally configured by ADR pin

TABLE 2. Control Registers

	D7	D6	D5	D4	D3	D2	D1	D0
Mono Volume control	0	0	0	MD4	MD3	MD2	MD1	MD0
Left Volume control	0	1	LD5	LD4	LD3	LD2	LD1	LD0
Right Volume control	1	0	RD5	RD4	RD3	RD2	RD1	RD0
Mode control	1	1	CD5	0	CD3	CD2	CD1	CD0

TABLE 3. Mono Volume Control

MD4	MD3	MD2	MD1	MD0	Gain (dB)
0	0	0	0	0	-34.5
0	0	0	0	1	-33.0
0	0	0	1	0	-31.5
0	0	0	1	1	-30.0
0	0	1	0	0	-28.5
0	0	1	0	1	-27.0
0	0	1	1	0	-25.5
0	0	1	1	1	-24.0
0	1	0	0	0	-22.5
0	1	0	0	1	-21.0
0	1	0	1	0	-19.5
0	1	0	1	1	-18.0
0	1	1	0	0	-16.5
0	1	1	0	1	-15.0
0	1	1	1	0	-13.5
0	1	1	1	1	-12.0
1	0	0	0	0	-10.5
1	0	0	0	1	-9.0
1	0	0	1	0	-7.5
1	0	0	1	1	-6.0
1	0	1	0	0	-4.5
1	0	1	0	1	-3.0
1	0	1	1	0	-1.5
1	0	1	1	1	0.0
1	1	0	0	0	1.5
1	1	0	0	1	3.0
1	1	0	1	0	4.5
1	1	0	1	1	6.0
1	1	1	0	0	7.5
1	1	1	0	1	9.0
1	1	1	1	0	10.5
1	1	1	1	1	12.0

TABLE 4. Stereo Volume Control

LD4//RD4	LD3//RD3	LD2//RD2	LD1//RD1	LD0//RD0	Gain (dB)
0	0	0	0	0	-40.5
0	0	0	0	1	-39.0
0	0	0	1	0	-37.5
0	0	0	1	1	-36.0
0	0	1	0	0	-34.5
0	0	1	0	1	-33.0
0	0	1	1	0	-31.5
0	0	1	1	1	-30.0
0	1	0	0	0	-28.5
0	1	0	0	1	-27.0
0	1	0	1	0	-25.5
0	1	0	1	1	-24.0
0	1	1	0	0	-22.5
0	1	1	0	1	-21.0
0	1	1	1	0	-19.5
0	1	1	1	1	-18.0
1	0	0	0	0	-16.5
1	0	0	0	1	-15.0
1	0	0	1	0	-13.5
1	0	0	1	1	-12.0
1	0	1	0	0	-10.5
1	0	1	0	1	-9.0
1	0	1	1	0	-7.5
1	0	1	1	1	-6.0
1	1	0	0	0	-4.5
1	1	0	0	1	-3.0
1	1	0	1	0	-1.5
1	1	0	1	1	0.0
1	1	1	0	0	1.5
1	1	1	0	1	3.0
1	1	1	1	0	4.5
1	1	1	1	1	6.0

TABLE 5. Mixer and Output Mode

Mode	CD3	CD2	CD1	CD0	Loudspeaker L	Loudspeaker R	Headphone L	Headphone R
0	0	0	0	0	SD	SD	SD	SD
1	0	0	0	1	RESERVED			
2	0	0	1	0	$2(G_M \times M)$	$2(G_M \times M)$	MUTE	MUTE
3	0	0	1	1	$2(G_M \times M)$	$2(G_M \times M)$	$(G_M \times M)$	$(G_M \times M)$
4	0	1	0	0	SD	SD	$(G_M \times M)$	$(G_M \times M)$
5	0	1	0	1	RESERVED			
6	0	1	1	0	RESERVED			
7	0	1	1	1	$2(G_L \times L)$	$2(G_R \times R)$	MUTE	MUTE
8	1	0	0	0	$2(G_L \times L)$	$2(G_R \times R)$	$(G_L \times L)$	$(G_R \times R)$
9	1	0	0	1	SD	SD	$(G_L \times L)$	$(G_R \times R)$
10	1	0	1	0	RESERVED			
11	1	0	1	1	RESERVED			
12	1	1	0	0	$2(G_L \times L) + 2(G_M \times M)$	$2(G_R \times R) + 2(G_M \times M)$	MUTE	MUTE
13	1	1	0	1	$2(G_L \times L) + 2(G_M \times M)$	$2(G_R \times R) + 2(G_M \times M)$	$(G_L \times L) + (G_M \times M)$	$(G_R \times R) + (G_M \times M)$
14	1	1	1	0	SD	SD	$(G_L \times L) + (G_M \times M)$	$(G_R \times R) + (G_M \times M)$
15	1	1	1	1	RESERVED			

M - M_{IN} Input Level
L - L_{IN} Input Level
R - R_{IN} Input Level
G_M - Mono Volume Control Gain
G_L - Left Stereo Volume Control Gain
G_R - Right Stereo Volume Control Gain
SD - Shutdown
MUTE - Mute

TABLE 6. National 3D Enhancement

LD5	0	Loudspeaker National 3D Off
	1	Loudspeaker National 3D On
RD5	0	Headphone National 3D Off
	1	Headphone National 3D On

TABLE 7. Wake-up Time Select

CD5	0	Fast Wake-up Setting
	1	Slow Wake-up Setting

I^2C COMPATIBLE INTERFACE

The LM4844 uses a serial bus, which conforms to the I^2C protocol, to control the chip's functions with two wires: clock (SCL) and data (SDA). The clock line is uni-directional. The data line is bi-directional (open-collector). The maximum clock frequency specified by the I^2C standard is 400kHz. In this discussion, the master is the controlling microcontroller and the slave is the LM4844.

The I^2C address for the LM4844 is determined using the ADR pin. The LM4844's two possible I^2C chip addresses are of the form $111110X_10$ (binary), where $X_1 = 0$, if ADR is logic low; and $X_1 = 1$, if ADR is logic high. If the I^2C interface is used to address a number of chips in a system, the LM4844's chip address can be changed to avoid any possible address conflicts.

The bus format for the I^2C interface is shown in Figure 2. The bus format diagram is broken up into six major sections:

The "start" signal is generated by lowering the data signal while the clock signal is high. The start signal will alert all devices attached to the I^2C bus to check the incoming address against their own address.

The 8-bit chip address is sent next, most significant bit first. The data is latched in on the rising edge of the clock. Each address bit must be stable while the clock level is high.

After the last bit of the address bit is sent, the master releases the data line high (through a pull-up resistor). Then the master sends an acknowledge clock pulse. If the LM4844 has received the address correctly, then it holds the data line low during the clock pulse. If the data line is not held low during the acknowledge clock pulse, then the master should abort the rest of the data transfer to the LM4844.

The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable high.

After the data byte is sent, the master must check for another acknowledge to see if the LM4844 received the data.

If the master has more data bytes to send to the LM4844, then the master can repeat the previous two steps until all data bytes have been sent.

The "stop" signal ends the transfer. To signal "stop", the data signal goes high while the clock signal is high. The data line should be held high when not in use.

I^2C INTERFACE POWER SUPPLY PIN (I^2CV_{DD})

The LM4844's I^2C interface is powered up through the I^2CV_{DD} pin. The LM4844's I^2C interface operates at a voltage level set by the I^2CV_{DD} pin which can be set independent to that of the main power supply pin V_{DD}. This is ideal whenever logic levels for the I^2C interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the main battery of a portable system.

NATIONAL 3D ENHANCEMENT

The LM4844 features a 3D audio enhancement effect that widens the perceived soundstage from a stereo audio signal. The 3D audio enhancement improves the apparent stereo channel separation whenever the left and right speakers are too close to one another, due to system size constraints or equipment limitations.

An external RC network, shown in Figure 1, is required to enable the 3D effect. There are separate RC networks for both the stereo loudspeaker outputs as well as the stereo headphone outputs, so the 3D effect can be set independently for each set of stereo outputs.

The amount of the 3D effect is set by the R_{3D} resistor. Decreasing the value of R_{3D} will increase the 3D effect. The C_{3D} capacitor sets the low cutoff frequency of the 3D effect. Increasing the value of C_{3D} will decrease the low cutoff frequency at which the 3D effect starts to occur, as shown by Equation 1.

$$f_{3D(-3dB)} = 1 / 2\pi(R_{3D})(C_{3D}) \quad (1)$$

Activating the 3D effect will cause an increase in gain by a multiplication factor of $(1 + 20k\Omega/R_{3D})$. Setting R_{3D} to $20k\Omega$ will result in a gain increase by a multiplication factor of $(1 + 20k\Omega/20k\Omega) = 2$ or 6dB whenever the 3D effect is activated. The volume control can be programmed through the I^2C compatible interface to compensate for the extra 6dB increase in gain. For example, if the stereo volume control is set at 0dB (11011 from Table 4) before the 3D effect is activated, the volume control should be programmed to –6dB (10111 from Table 4) immediately after the 3D effect has been activated. Setting $R_{3D} = 20k\Omega$ and $C_{3D} = 0.22\mu F$ allows the LM4844 to produce a pronounced 3D effect with a minimal increase in output noise.

OUTPUT CAPACITOR-LESS (OCL) OPERATION AND LAYOUT TECHNIQUES FOR OPTIMUM CROSSTALK

The LM4844's OCL headphone architecture eliminates output coupling capacitors. Unless the headphone is in shutdown, the OCL output will be at a bias voltage of $½V_{DD}$, which is applied to the stereo headphone jack's sleeve. This voltage matches the bias voltage present on LHP and RHP outputs that drive the headphones. The headphones operate in a manner similar to a bridge-tied load (BTL). Because the same DC voltage is applied to both headphone speaker terminals there is no net DC current flow through the speaker. AC current flows through a headphone speaker as an audio signal's output amplitude increases on the speaker's terminal.

The headphone jack's sleeve is not connected to circuit ground when used in OCL mode. Using the headphone output jack as a line-level output will place the LM4844's $½V_{DD}$ bias voltage on a plug's sleeve connection.

Since the LHP and RHP outputs of the LM4844 share the OCL output as a reference, certain layout techniques should be used in order to achieve optimum crosstalk performance. The crosstalk will depend on the parasitic resistance of the trace connecting the LM4844 OCL output to the headphone jack sleeve and on the load resistance value. Since the load resistance is often predetermined, it is advisable to use a trace that is as short and as wide as possible. Reasonable application of this layout technique will result in crosstalk values of 60dB, as specified in the electrical characteristics table.

BRIDGE CONFIGURATION EXPLANATION

The LM4844 consists of two sets of bridged-tied amplifier pairs that drive the left loudspeaker (LLS) and the right loudspeaker (RLS). For this discussion, only the LLS bridge-tied amplifier pair will be referred to. The LM4844 drives a load, such as a speaker, connected between outputs, LLS+ and LLS-. In the LLS amplifier block, the output of the amplifier that drives LLS- serves as the input to the unity gain inverting amplifier that drives LLS+.

This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between LLS- and LLS+ and driven differentially (commonly referred to as 'bridge mode'). This results in a differential or BTL gain of:

$$A_{VD} = 2(R_f / R_i) = 2 \quad (2)$$

Both the feedback resistor, R_f, and the input resistor, R_i, are internally set.

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. Theoretically, this produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited and that the output signal is not clipped.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing LLS- and LLS+ outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a typical single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier.

A direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation. The LM4844 has 2 sets of bridged-tied amplifier pairs driving LLS and RLS. The maximum internal power dissipation operating in the bridge mode is twice that of a single-ended amplifier. From Equation (3) and (4), assuming a 5V power supply and an 8Ω load, the maximum power dissipation for LLS and RLS is 634mW per channel.

$$P_{DMAX-LLS} = 4(V_{DD})^2 / (2\pi^2 R_L)\text{: Bridged} \quad (3)$$

$$P_{DMAX-RLS} = 4(V_{DD})^2 / (2\pi^2 R_L)\text{: Bridged} \quad (4)$$

The LM4844 also has a pair of single-ended amplifiers driving LHP and RHP. The maximum internal power dissipation for ROUT and LOUT is given by equation (5) and (6). From Equations (5) and (6), assuming a 5V power supply and a 32Ω load, the maximum power dissipation for LOUT and ROUT is 40mW per channel.

$$P_{DMAX-LHP} = (V_{DD})^2 / (2\pi^2 R_L)\text{: Single-ended} \quad (5)$$

$$P_{DMAX-RHP} = (V_{DD})^2 / (2\pi^2 R_L)\text{: Single-ended} \quad (6)$$

The maximum internal power dissipation of the LM4844 occurs during output modes 3, 8, and 13 when both loudspeaker and headphone amplifiers are simultaneously on; and is given by Equation (7).

$$P_{DMAX-TOTAL} = P_{DMAX-LLS} + P_{DMAX-RLS} + P_{DMAX-LHP} + P_{DMAX-RHP} \quad (7)$$

The maximum power dissipation point given by Equation (7) must not exceed the power dissipation given by Equation (8):

$$P_{DMAX}' = (T_{JMAX} - T_A) / \theta_{JA} \quad (8)$$

The LM4844's T_{JMAX} = 150°C. In the TL package, the LM4844's θ_{JA} is 62°C/W. At any given ambient temperature T_A, use Equation (8) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (8) and substituting $P_{DMAX-TOTAL}$ for P_{DMAX}' results in Equation (9). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4844's maximum junction temperature.

$$T_A = T_{JMAX} - P_{DMAX-TOTAL}\,\theta_{JA} \quad (9)$$

For a typical application with a 5V power supply, stereo 8Ω loudspeaker load, and the stereo 32Ω headphone load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 100°C for the TL package.

$$T_{JMAX} = P_{DMAX-TOTAL}\,\theta_{JA} + T_A \quad (10)$$

Equation (10) gives the maximum junction temperature T_{JMAX}. If the result violates the LM4844's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases. If the result of Equation (7) is greater than that of Equation (8), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction-to-case thermal impedance, θ_{CS} is the case-to-sink thermal impedance, and θ_{SA} is the sink-to-ambient thermal impedance.) Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0µF tantalum bypass capacitance connected between the LM4844's supply pins and ground. Keep the length of leads and traces that connect capacitors between the LM4844's power supply pin and ground as short as possible.

SELECTING EXTERNAL COMPONENTS

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires a high value input coupling capacitor (C_i in Figure 1). In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 50Hz. Applications using speakers with this limited frequency response reap little improvement; by using a large input capacitor.

The internal input resistor (R_i) and the input capacitor (C_i) produce a high pass filter cutoff frequency that is found using Equation (13).

$$f_c = 1 / (2\pi R_i C_i) \quad (11)$$

As an example when using a speaker with a low frequency limit of 50Hz and $R_i = 20k\Omega$, C_i, using Equation (13) is 0.19µF. The 0.22µF C_i shown in Figure 4 allows the LM4844 to drive high efficiency, full range speaker whose response extends below 40Hz.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_B, the capacitor connected to the BYPASS pin. Since C_B determines how fast the LM4844 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4844's outputs ramp to their quiescent DC voltage (nominally $V_{DD}/2$), the smaller the turn-on pop. Choosing C_B equal to 2.2µF along with a small value of C_i (in the range of 0.1µF to 0.39µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_i no larger than necessary for the desired bandwidth helps minimize clicks and pops. C_B's value should be in the range of 5 times to 10 times the value of C_i. This ensures that output transients are eliminated when the LM4844 transitions in and out of shutdown mode. Connecting a 2.2µF capacitor, C_B, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. However, increasing the value of C_B will increase wake-up time. The selection of bypass capacitor value, C_B, depends on desired PSRR requirements, click and pop performance, wake-up time, system cost, and size constraints.

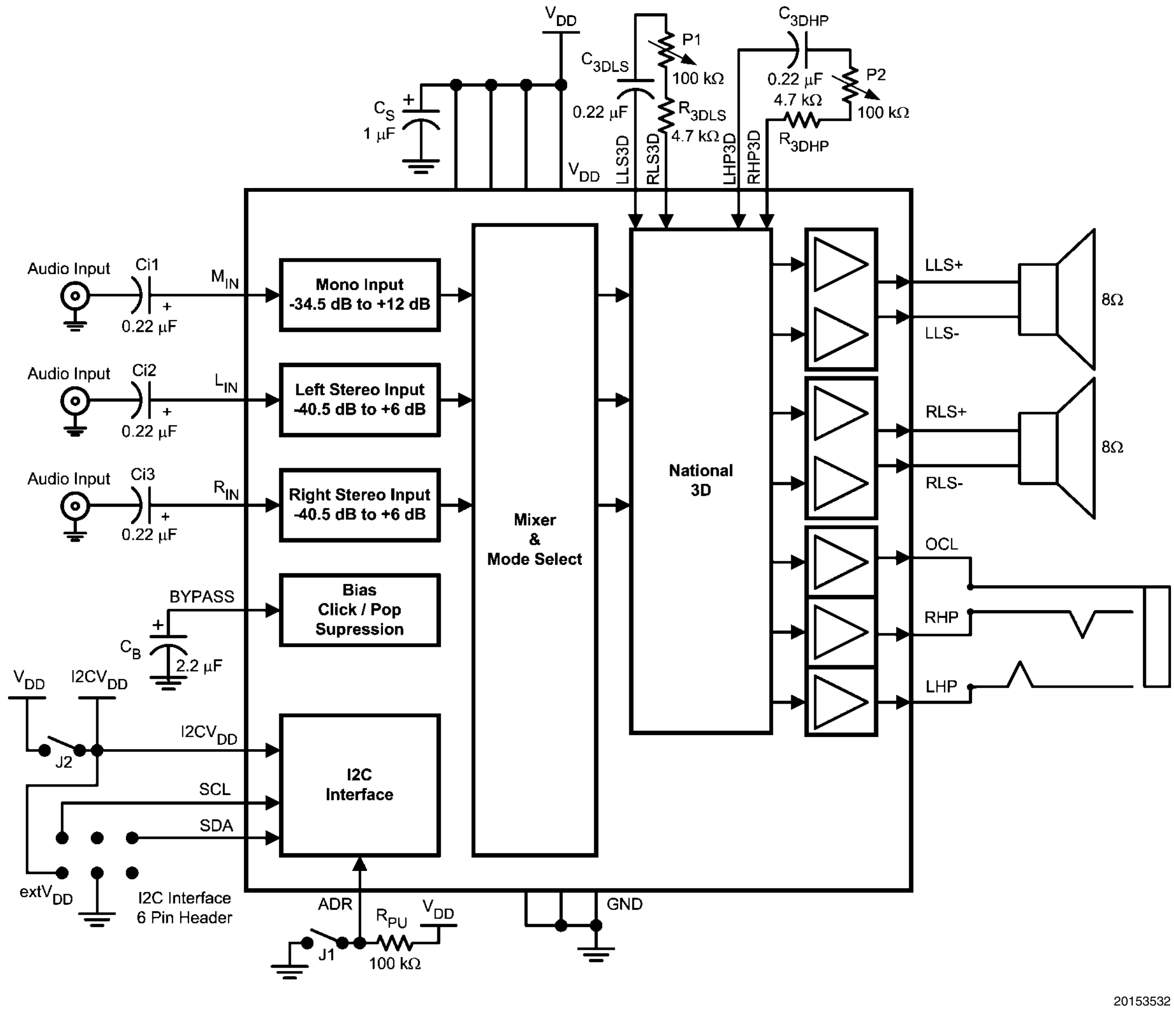
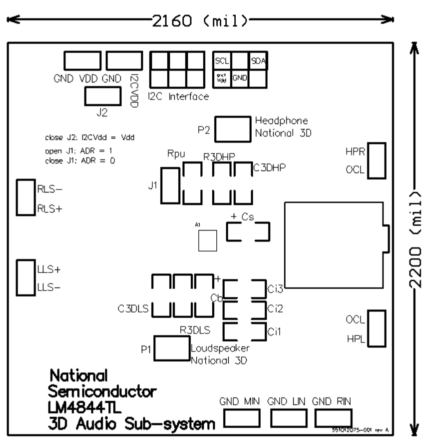


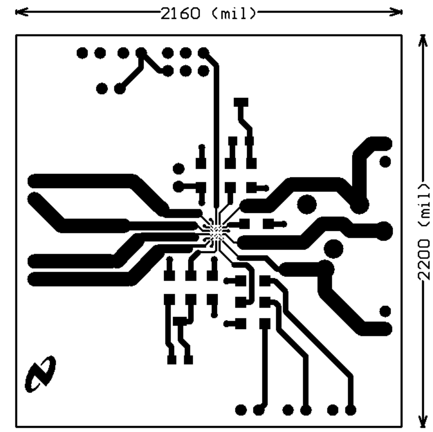
FIGURE 4. Reference Design Board Schematic

Demonstration Board Layout



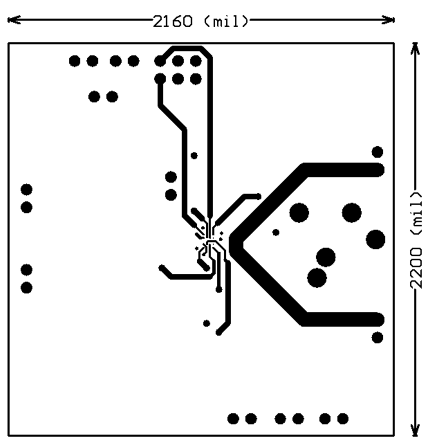
20153517

Recommended TL PCB Layout: Silkscreen Layer



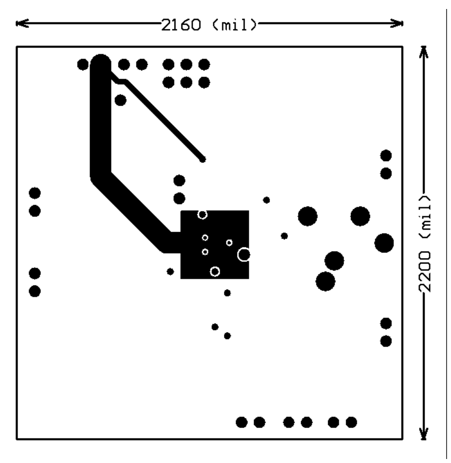
20153518

Recommended TL PCB Layout: Top Layer



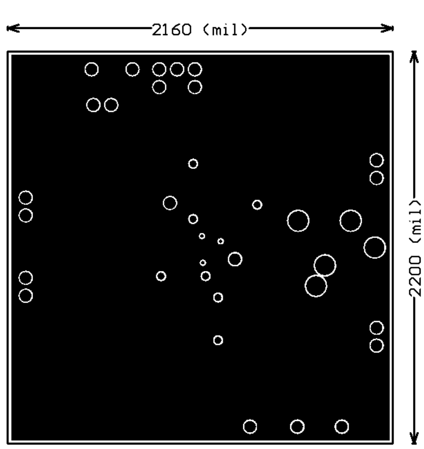
20153515

Recommended TL PCB Layout: Mid Layer 1



20153516

Recommended TL PCB Layout: Mid Layer 2



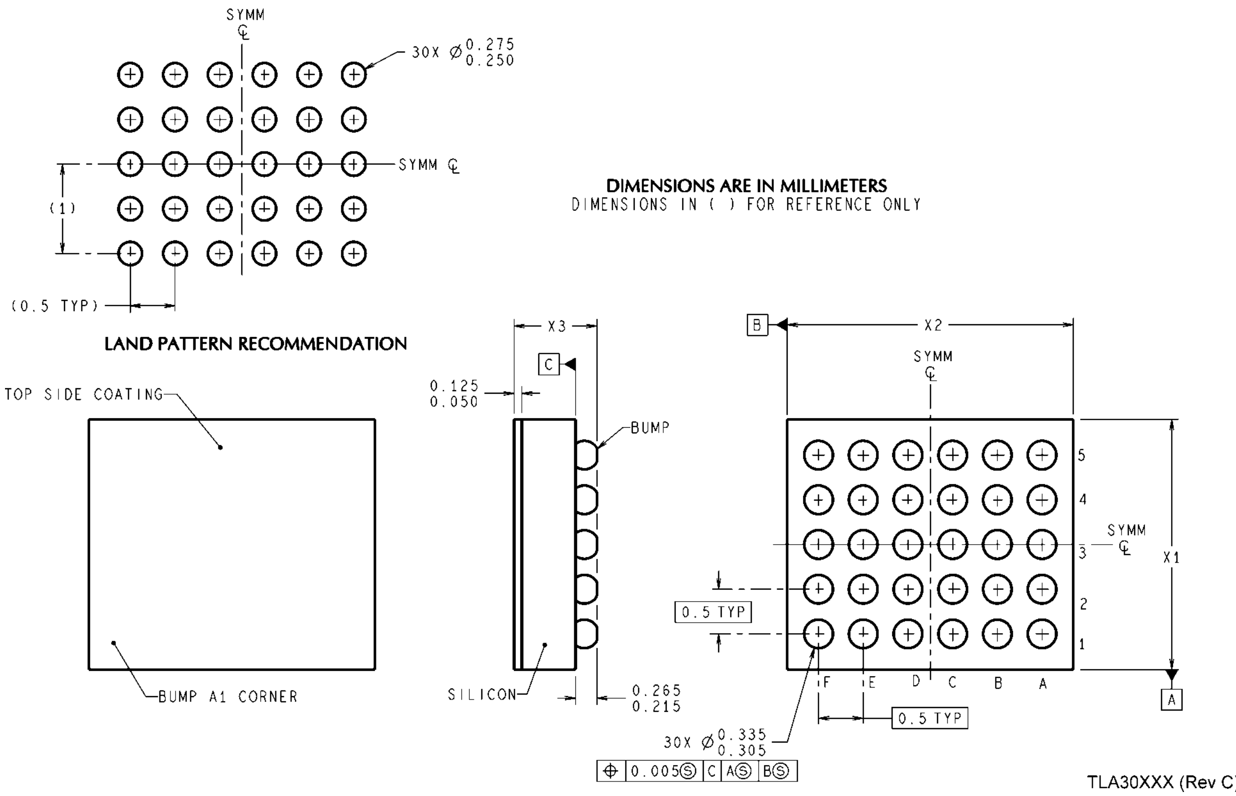
20153514

Recommended TL PCB Layout: Bottom Layer

Revision History

Rev	Date	Description
1.1	06/01/06	Initial WEB.
1.2	07/20/07	Edited the Control Interface Electrical Characteristics tables.
1.3	08/07/07	Changed the I^2CVdd from 1.8V into 1.7V (under the Operating Ratings).
1.4	08/23/07	Fixed one place of typo.

Physical Dimensions inches (millimeters) unless otherwise noted



30 Bump Micro SMD (TL) Package
Order Number LM4844TL
NS Package Number TLA30CZA
X1 = 2.543±0.03 X2 = 2.949±0.03 X3 = 0.6±0.075

Notes

Notes

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